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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/672,424	09/28/2000	GURJEET SINGH SAUND	114596-31-0127BS	7407

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EXAMINER

COLEMAN, ERIC

ART UNIT PAPER NUMBER

2183

DATE MAILED: 06/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/672,424	Applicant(s) SAUND ET AL.	
	Examiner Eric Coleman	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 March 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3-6,8,9 and 12-58 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1,14-53 and 55-58 is/are allowed.
- 6) ☒ Claim(s) 5,6,8,12,13 and 54 is/are rejected.
- 7) ☒ Claim(s) 3,4 and 9 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claim 5,6, and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Colwell (patent No. 5,729,728) in view of Papworth (patent No. 5,404,473) and Hammond (patent No. 5,638,525).

3. Colwell taught the invention substantially as claimed including a data processing ("DP") system comprising: Decoder (150) (e.g., see fig. 2) that receives a macroinstruction and decodes the macroinstruction into uopcode and [MU] field and microinstruction branch, static bit. Colwell taught the macroinstruction decoding produced a pattern of microinstructions implementing a basic operation (e.g., see fig.2) and col. 6, line 25-col. 7, line 14 and col. 12, line 61-col. 13, line 27). Colwell taught that the decoder transfers stream uops and issue up to three in order uops during each cycle (e.g., see col. 10, lines 27-32). Colwell taught that in the case of a branch instruction outcome is predicted (e.g., see col. 12, lines 7-35).

4. Colwell did not expressly detail (claim 5) that generating a plurality of iterations where a branch was predicted not taken. Papworth however taught the processing of loops including a number of loops specified by a macroinstruction by unrolling the loops into iterations each of which are conditionally executed (e.g., see col. 7, line 2-col.8, line

25). Papworth also taught a branch Cuop that was predicted not taken of the MS continued to stay in the loop until the MS loop counter was zero or conditional branch Cuop was mispredicted (e.g., see col. 11, lines 2-12).

5. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Colwell and Papworth. Both Colwell and Papworth were directed toward the processing instruction sequences that were conditionally executed. The incorporation of the Papworth teachings of unrolling loops would have allowed the combined system to more efficiently process sequences of instructions that were repeated by loading unrolled loop into the pipeline and when the end of the iterations occurred fewer pipeline stages would have been required to be flushed or discarded (e.g., see col. 9, lines 3-15 of Papworth).

6. As per claim 5, Colwell taught that the microinstruction set architecturally available and the branch instruction available to programs fetched from memory of the computer and branch prediction bits for use in the processing of microinstruction can be set by the microprogrammer (e.g., see col. 12, lines 19-23) The macroinstructions of Colwell are decoded and in response to the decoding of the macroinstructions the microinstructions are accessed. Also Colwell taught the use of a [Mu] bit that was part of the macroinstruction that indicated whether the instruction was to operated as a macroinstruction or microinstruction (e.g., see col. 11, lines 21-55) the Mu bit allows the architecture to selectively perform operations such as branches either as macroinstructions of microinstructions) (this provides for visibility of the microinstruction to the programs). On the other hand Hammond (patent taught a system with a

processor that executes programs that contain CISC and RISC instructions. Note RISC instructions are microinstructions.

7. One of ordinary skill in the art would have been motivated to incorporate the teachings of Hammond in system of Colwell and Papworth at least because the added ability to include each instruction of the microinstruction and microinstructions in programs allows the processor to accept multiple operating systems and instructions from multiple instruction sets (e.g., see col. 1, lines 49-52 of Hammond). This allows the user or programmer in the Colwell and Papworth system to directly use microinstruction taught by Colwell as determined by the decoding of macroinstructions. This also allows additional flexibility to the programmer or user in the implementation of the combined system and to tailor or fine tune or optimize applications.

8. As per claim 6, Colwell taught an instruction cache (103) and a victim cache (105) (e.g., see fig. 1). Colwell did not however particularize the memory management between memory and cache. The use of external memory for storing data and instruction that are not currently being used and providing a memory management to provide at least coherency of the data in the external memory and cache was well known in the art at the time of the claimed invention. One of ordinary skill in the art would have been motivated to provide a memory management and external memory to allow the system to readily access large amounts of data and instructions as needed by the currently running program and memory management provide control to determine whether the data in the external memory and cache is valid. On the other hand Papworth taught fetching instructions from the cache and upon a cache miss fetching

instructions from external memory and the system comprising an data cache controller (203) and a bus controller that manages transfers and data and cache coherency.

9. As per claim 54, Colwell taught the branch microinstruction is generated carrying a marker indicating that the branch microinstruction defines the boundary(beginning or end of an iteration or a sequence of microinstructions (e.g., see col. 10, lines 18-26 of Colwell). When the instruction would have been part of an unrolled loop iteration as taught by Papworth these beginning and ending markers would have provided a boundary between iterations. As to whether when the markers were used for an instruction not at the end or beginning. Clearly since the instruction in Colwell could be one of a beginning or ending without being both. Therefore the Colwell system would have been able "turn off" a beginning or ending indicator. One of ordinary skill incorporated in the Colwell markers into the Papworth unrolled loops would have been motivated to "turnoff" both markers as appropriate when the instruction was not at the end or beginning of a series unrolled loops.

10. Claim 8,13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Colwell (patent No. 5,729,728) in view of Papworth (patent No. 5,404,473).

11. Colwell taught the invention substantially as claimed including a data processing ("DP") system comprising: Decoder(150) (e.g., see fig. 2) that receives a macroinstruction and decodes the macroinstruction into uopcode and [MU] field and microinstruction branch, static bit. Colwell taught the macroinstruction decoding produced a pattern of microinstructions implementing a basic operation (e.g., see fig.2) and col. 6, line 25-col. 7, line 14 and col. 12, line 61-col. 13, line 27). Colwell taught that

the decoder transfers stream uops and issue up to three in order uops during each cycle (e.g., see col. 10, lines 27-32). Colwell taught that in the case of a branch instruction outcome is predicted (e.g., see col. 12, lines 7-35).

12. Colwell did not expressly detail (claim 13) that generating a plurality of iterations where a branch was predicted not taken. Papworth however taught the processing of loops including a number of loops specified by a macroinstruction by unrolling the loops into iterations each of which are conditionally executed (e.g., see col. 7, line 2-col.8, line 25). Papworth also taught a branch Cuop that was predicted not taken of the MS continued to stay in the loop until the MS loop counter was zero or conditional branch Cuop was mispredicted (e.g., see col. 11, lines 2-12).

13. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Colwell and Papworth. Both Colwell and Papworth were directed toward the processing instruction sequences that were conditionally executed. The incorporation of the Papworth teachings of unrolling loops would have allowed the combined system to more efficiently process sequences of instructions that were repeated by loading unrolled loop into the pipeline and when the end of the iterations occurred fewer pipeline stages would have been required to be flushed or discarded (e.g., see col. 9, lines 3-15 of Papworth).

14. As per claim 13, Papworth taught ceasing to generate iterations when a condition of the macroinstruction is detected (e.g., see col. 7, line 24-col. 8, line 25) that comprises a branch mispredict (e.g., see col. 9, lines 3-15) as when the number of iterations is too many the extra iterations are executed as NOOP operations.

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15. As per claim 13, Colwell taught the branch microinstruction is generated carrying a marker indicating that the branch microinstruction defines a boundary (beginning or ending of an iteration (e.g., see col. 10, lines 18-26 of Colwell). When the instruction would have been part of an unrolled loop iteration as taught by Papworth these beginning and ending markers would have provided a boundary between iterations. As to whether when the markers were used for an instruction not at the end or beginning. Clearly since the instruction in Colwell could be one of a beginning or ending without being both. Therefore the Colwell system would have been able "turn off" a beginning or ending indicator. One of ordinary skill incorporated in the Colwell markers into the Papworth unrolled loops would have been motivated to "turnoff" both markers as appropriate when the instruction was not at the end or beginning of a series unrolled loops.

16. As per claim 8 the macroinstructions of Colwell are decoded and in response to the decoding of the macroinstructions the microinstructions are accessed. Also Colwell taught the use of a [Mu] bit that was part of the macroinstruction that indicated whether the instruction was to operate as a macroinstruction or microinstruction (e.g., see col. 11, lines 21-55) the Mu bit allows the architecture to selectively perform operations such as branches either as macroinstructions of microinstructions) (this provides for visibility of the microinstruction to the programs and operation and storing of instructions of both macro and microinstruction set). Since the location of microinstruction (or data therefore) in a location intended to store macroinstruction an vis versa could provide

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incorrect operation of the system one of ordinary skill would have been motivated to invalidate and data in memory data stored in the incorrect memory.

17. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Colwell and Papworth as applied to claim 13 above, and further in view of Hammond (patent No. 5,638,525).

18. As per claim 12, Colwell taught that the microinstruction set architecturally available and the branch instruction available to programs fetched from memory of the computer and branch prediction bits for use in the processing of microinstruction can be set by the microprogrammer (e.g., see col. 12, lines 19-23) The macroinstructions of Colwell are decoded and in response to the decoding of the macroinstructions the microinstructions are accessed. Also Colwell taught the use of a [Mu] bit that was part of the macroinstruction that indicated whether the instruction was to operate as a macroinstruction or microinstruction (e.g., see col. 11, lines 21-55) the Mu bit allows the architecture to selectively perform operations such as branches either as macroinstructions or microinstructions). On the other hand Hammond (patent taught a system with a processor that executes programs that contain CISC and RISC instructions. Note RISC instructions are microinstructions.

19. One of ordinary skill in the art would have been motivated to incorporate the teachings of Hammond in system of Colwell and Papworth at least because the added ability to include each instruction of the microinstruction and microinstructions in programs allows the processor to accept multiple operating systems and instructions from multiple instruction sets (e.g., see col. 1, lines 49-52 of Hammond). This allows the

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user of programmer in the Colwell and Papworth system to directly use microinstruction taught by Colwell as determined by the decoding of macroinstructions. This also allows additional flexibility to the programmer or user in the implementation of the combined system and to tailor or fine tune or optimize applications.

Allowable Subject Matter

20. Claims 3,4,9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

21. Claims 1,14-53,55-58 are allowed.

Response to Arguments

22. Applicant's arguments with respect to claims 5,6,8,9,12 and 13 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EC



ERIC COLEMAN
PRIMARY EXAMINER